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EXAMINER

TRAN, ANH Q

ART UNIT

PAPER NUMBER

2819

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Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
2. Claim 32 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Both the first-mentioned stage and the second-mentioned stage have third stage that is both a source stage and a destination stage. The recites limitations in the claim are very confusing and vague. Clarification is requires.
3. claims 33-37 are rejected as dependent on claim 32.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 9, 16-18, 19-20, 25-26, 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Young et al (6,107,827).

Young shows:

1. Logic module circuitry comprising: combinational logic circuitry having at least first (J, H), second (F5A, F6A), and third stages (MJ, MH); and XOR circuitry (SH, SJ)

interposed between two of the stages for logically combining a carry in signal (CIN1) with at least one combinational signal (H or J output) in the combinational logic circuitry.

3. the circuitry defined in claim 1 further comprising: circuitry for producing a carry out signal (CJ) from the carry in signal and combinational signals in the combinational logic circuitry (MJ or MH).

9. The circuitry defined in claim 1 wherein the XOR circuitry is interposed between the second and third stages.

16-18. The circuitry defined claim 1 wherein the first and second stages are programmable to produce an output signal that is usable in forming an arithmetic sum of first and second stage input signals, difference between first and second stage input signals or product of first and second stage input signals (inherent limitations, since function generators J, H, G, F are programmable to do these functions).

19. The circuitry defined in claim 18 wherein the third stage (MJ, MH) and the XOR circuitry are operable to form the arithmetic sum of the output signal, a third stage input signal (output O from H), and a carry in signal (CIN1).

20. A programmable logic device comprising logic module circuitry as defined in claim 1.

The apparatus described above is applicable to the method claims 25-26, 29-30.

Claim Rejections - 35 USC § 103

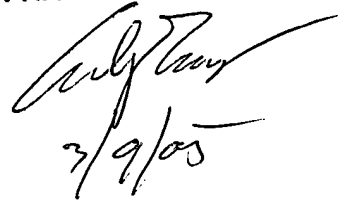
3. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (6,107,827) in view of Park et al (6,359,468).

Young discloses the claimed invention except for a memory, processing circuitry, and programmable logic device mounted on a printed circuit board. Park discloses a memory, processing circuitry, and programmable logic device mounted on a printed circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the programmable logic device of Young in a digital processing system of Park, in order to provide wide variety of applications where the advantage of using programmable logic device.

Allowable Subject Matter

4. Claims 2, 4-8, 10-15, 27-28, 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

ANH Q. TRAN
PRIMARY EXAMINER



3/9/05